REMARKS

The Applicant has carefully reviewed and considered the Examiner's Action mailed September 24, 2004, in which Claims 1-18 were indicated as being allowable over the prior art of record if amended to overcome the rejection under 35 U.S.C. §112, second paragraph. Reconsideration is respectfully requested in view of the foregoing amendments and the comments set forth below.

By this Amendment, the specification is amended to editorially revise the English translation and correct reference characters; Claims 1-5 and 7-18 are amended to overcome the issues raised on paragraph 3 of the Action; and a new Abstract of the Disclosure is presented on a separate sheet. Accordingly, indicated allowable claims 1-18 are pending in the present application.

The amendments to the claims are editorial in nature. Consequently, the scope of the claims remain unchanged. That is, the foregoing amendments to the claims are not narrowing amendments.

In view of the foregoing amendments and remarks, it is respectfully requested that the objection and rejections of record be withdrawn, and that a Notice of Allowance be issued indicating that claims 1-18 are allowable over the prior art of record.

Should the Examiner believe that a conference would advance the prosecution of this application, the Examiner is encouraged to telephone the undersigned counsel to arrange such a conference.

Respectfully submitted,

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Abstract of the Disclosure

A delay apparatus delays a rising edge and a falling edge of a digital signal. The delay apparatus includes a first edge detection circuit which detects a first edge or rising edge of the digital signal and generates a detection signal; a set circuit that includes a first counter for generating a count value and clearing the count value in response to the detection signal, wherein the set circuit generates a set signal if the count value reaches the number of the reference clock signals corresponding to the delay period of time; a reset circuit which generates a reset signal if an elapsed period of time since a generation of the set signal equals a period of time the digital signal maintains the second logic level; and an output circuit that outputs a delayed digital signal including edges synchronized with the set signal and the reset signal.